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2	US 20020093032		US-PGPU	20020718	59
3	US 6680867 B2		USPAT	20040120	55
4	US 6563743 B2		USPAT	20030513	57

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US006563743B2

(12) **United States Patent**
Hanzawa et al.

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(45) Date of Patent: **May 13, 2003**

(54) SEMICONDUCTOR DEVICE HAVING DUMMY CELLS AND SEMICONDUCTOR DEVICE HAVING DUMMY CELLS FOR REDUNDANCY

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(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

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(52) U.S. Cl. 365/189.03; 365/230.02; 365/189.01

(58) Field of Search 365/189.02, 230.02, 365/189.04, 210, 189.01, 196, 225

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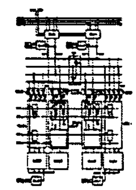
(57) ABSTRACT

A dummy cell includes a plurality of first memory cells MC for storing "1" or "0", arranged at points of intersection between a plurality of word lines WR0 to WR7 and a plurality of first data lines D0 to D7, a plurality of first dummy cells MCH for storing "1" or "0", arranged at points of intersection between the word lines WR0 to WR7 and a first dummy data line, and a plurality of second dummy cells MCL for storing "0", arranged at points of intersection between the word lines WR0 to WR7 and a second dummy data line DD1.

22 Claims, 29 Drawing Sheets



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